The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed over said second insulating film.

2. (Original) A semiconductor device of claim 1 wherein said semiconductor layer comprises crystalline silicon.

3. (Previously Presented) A semiconductor device of claim 1 wherein said first inorganic insulating film comprises silicon oxide.

4. (Original) A semiconductor device of claim 1 wherein said second insulating film comprises polyimide.

5. (Original) A semiconductor device of claim 1 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

6. (Original) A semiconductor device of claim 1 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

7. (Previously Presented) A semiconductor device of claim 1 wherein a portion of said pixel electrode is located under said electrode.

8. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed over said second insulating film.

9. (Original) A semiconductor device of claim 8 wherein said semiconductor layer comprises crystalline silicon.

10. (Previously Presented) A semiconductor device of claim 8 wherein said first inorganic insulating film comprises silicon oxide.

11. (Original) A semiconductor device of claim 8 wherein said second insulating film comprises polyimide.

12. (Original) A semiconductor device of claim 8 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

13. (Original) A semiconductor device of claim 8 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

14. (Previously Presented) A semiconductor device of claim 8 wherein a portion of said pixel electrode is located under said electrode.

15. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed over said second insulating film.

16. (Original) A semiconductor device of claim 15 wherein said semiconductor layer comprises crystalline silicon.

17. (Previously Presented) A semiconductor device of claim 15 wherein said first inorganic insulating film comprises silicon oxide.

18. (Original) A semiconductor device of claim 15 wherein said second insulating film comprises polyimide.

19. (Original) A semiconductor device of claim 15 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film compromising titanium nitride.

20. (Original) A semiconductor device of claim 15 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

21. (Previously Presented) A semiconductor device of claim 15 wherein a portion of said pixel electrode is located under said electrode.

22. (Original) A semiconductor device of claim 15 wherein said transparent pixel electrode comprises indium tin oxide.

23. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed over said second insulating film.

24. (Original) A semiconductor device of claim 23 wherein said semiconductor layer comprises crystalline silicon.

25. (Previously Presented) A semiconductor device of claim 23 wherein said first inorganic insulating film comprises silicon oxide.

26. (Original) A semiconductor device of claim 23 wherein said second insulating film comprises polyimide.

27. (Original) A semiconductor device of claim 23 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

28. (Original) A semiconductor device of claim 23 wherein said pixel electrode is electrically connected to one of said first and second impurity regions.

29. (Previously Presented) A semiconductor device of claim 23 wherein a portion of said pixel electrode is located under said electrode.

30. (Previously Presented) A semiconductor device of claim 23 wherein said transparent pixel electrode comprises indium tin oxide.

31. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said

semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions, wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions.

32. (Original) A semiconductor device of claim 31 wherein said semiconductor layer comprises crystalline silicon oxide.

33. (Previously Presented) A semiconductor device of claim 31 wherein said first inorganic insulating film comprises silicon oxide.

34. (Original) A semiconductor device of claim 31 wherein said second insulating film comprises polyimide.

35. (Original) A semiconductor device of claim 31 wherein said second conductive film comprises titanium nitride.

36. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions, wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions.

37. (Original) A semiconductor device of claim 36 wherein said semiconductor layer comprises crystalline silicon.

38. (Previously Presented) A semiconductor device of claim 36 wherein said first inorganic insulating film comprises silicon oxide.

39. (Original) A semiconductor device of claim 36 wherein said second insulating film comprises polyimide.

40. (Original) A semiconductor device of claim 36 wherein said second conductive film comprises titanium nitride.

41. (Original) A semiconductor device of claim 36 wherein said transparent pixel electrode comprises indium tin oxide.

42. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions, wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions, wherein said electrode comprises a same material as said conductive layer.

43. (Original) A semiconductor device of claim 42 wherein said semiconductor layer comprises crystalline silicon.

44. (Previously Presented) A semiconductor device of claim 42 wherein said first inorganic insulating film comprises silicon oxide.

45. (Original) A semiconductor device of claim 42 wherein said second insulating film comprises polyimide.

46. (Original) A semiconductor device of claim 42 wherein said second conductive film comprises titanium nitride.

47. (Original) A semiconductor device of claim 42 wherein said transparent pixel electrode comprises indium tin oxide.

48. (Currently Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface, ~~wherein said channel region is formed so as to exclude a region where a catalyst element is introduced~~ wherein said semiconductor layer contains a catalyst element at a concentration of 1×10^{19} atoms/cm^3 or less;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film formed over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions;

a pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions,

wherein a portion of said pixel electrode is located below said electrode.

49. (Previously Presented) A semiconductor device of claim 48 wherein said semiconductor layer comprises crystalline silicon.

50. (Previously Presented) A semiconductor device of claim 48 wherein said first inorganic insulating film comprises silicon oxide.

51. (Previously Presented) A semiconductor device of claim 48 wherein said second insulating film comprises polyimide.

52. (Previously Presented) A semiconductor device of claim 48 wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising titanium nitride.

53. (Previously Presented) A semiconductor device of claim 1 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

54. (Previously Presented) A semiconductor device of claim 8 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

55. (Previously Presented) A semiconductor device of claim 15 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

56. (Previously Presented) A semiconductor device of claim 23 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

57. (Previously Presented) A semiconductor device of claim 31 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

58. (Previously Presented) A semiconductor device of claim 36 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

59. (Previously Presented) A semiconductor device of claim 42 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.

60. (Previously Presented) A semiconductor device of claim 48 wherein said catalyst element is one selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, P, As, and Sb.